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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of: **Shinichiroh IKEMASU, et al.**

Group Art Unit: **2814**

Serial No.: **10/050,169**

Examiner: **WEISS, Howard**

Filed: **January 18, 2002**

Confirmation No.: **9818**

For: **HIGHLY INTEGRATED AND RELIABLE DRAM AND ITS MANUFACTURE**

INFORMATION DISCLOSURE STATEMENT
PURSUANT TO 37 CFR 1.97(b)(4)

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

March 19, 2004

Sir:

The attention of the Patent and Trademark Office is hereby directed to the documents listed on the attached Form PTO-1449. The documents were made of record in related application Serial No. 10/166,620, filed June 12, 2002.

The above information is presented so that the Patent and Trademark Office can, in the first instance, determine any materiality thereof to the claimed invention. See 37 CFR 1.104(a) concerning the PTO duty to consider and use any such information. It is respectfully requested that the information be expressly considered during the prosecution of this application, and that the documents cited in the attached Form PTO-1449 be made of record therein and appear on the first page of any patent to issue therefrom.

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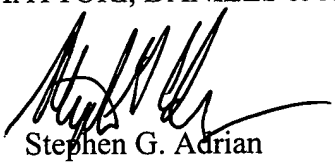
The Commissioner is authorized to charge our Deposit Account No. 50-2866 for any fee which is deemed by the Patent and Trademark Office to be required to effect consideration of this statement.

Respectfully submitted,

WESTERMAN, HATTORI, DANIELS & ADRIAN, LLP



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SGA/arf
Enclosures: PTO-1449 and 18 References

Attorney Docket No.**970607B**

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INFORMATION DISCLOSURE CITATION PTO-1449	Atty. Docket No. **970607B**	Serial No. **10/050,169**
	Applicant(s): **Shinichiroh IKEMASU et al.**	
	Filing Date: **January 18, 2002**	Group Art Unit: **2814**

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U.S. PATENT DOCUMENTS

Examiner Initial		Document No.	Name	Date	Class	Subclass	Filing Date (If appropriate)
_____	AA	5,605,857	Jost et al.	02/97			
_____	AB	5,324,681	Lowrey et al.	06/94			
_____	AC	5,292,677	Dennison	03/94			
_____	AD	5,281,549	Fazan et al.	01/94			
_____	AE	5,760,429	Yano et al.	6/98			
_____	AF	5,479,054	Tottori	12/95			
_____	AG	5,150,278	Gonzallez et al.	9/92			
_____	AH						
_____	AI						
_____	AJ						
_____	AK						
_____	AL						
_____	AM						
_____	AN						
_____	AO						

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OTHER DOCUMENTS

_____	AP	B.LUTHER et al.; Planar Copper-Polyimide Back End of the Line"; Proceedings of 10th International VMIC; pages 15-21; June 1993.
_____	AQ	B.M. SOMERO et al.; "A Modular in-situ Integration Scheme for Deep Submicron", Proceedings of 10th International VMIC; pages 28-34; June 1993.
_____	AR	M.F. CHISHOLM et al.; "A High Performance 0.5 um Five-Level Metal Process with Extendibility of Sub-Half Micron"; pages 22-28; June 1994.
_____	AS	M. RUTTEN et al.; "Pattern Density Effects in Tungsten CMP", Proceedings of 12th International VMIC; pages 491-497; June 1995.
_____	AT	I. NAIKI et al.; "Center Wordline Cell: A New Symmetric Layout Cell for 64Mb SRAM"; Technical Digest of IEDM; pages 817-820; December 1993.
_____	AU	T. KAGA et al.; "A 0.29-um2 MIM-Crown Cell and Process Technologies for 1-Gigabit DRAMs"; Technical Digest of IEDM; pages 927-929; December 1994.
_____	AV	H.K. KANG et al.; "Highly Manufacturable Process Technology for Reliable 256 Mbit and 1 Gbit DRAMs"; Technical Digest of IEDM; pages 635-638; December 1994.
_____	AW	Y. OHJI et al.; "Ta_2O_5 Capacitors Dielectric Material for Giga-bit DRAMs"; Technical Digest of IEDM; pages 111-114; December 1995.
_____	AX	Y. NISHIOKA et al.; "Giga-bit Scale DRAM Cell with New Simple Ru/(Ba,Sr)TiO3/Ru Stacked Capacitors Using X-ray Lithography"; Technical Digest of IEDM; pages 903-906; December 1995.
_____	AY	K.P. LEE et al.; "A Process Technology for 1 Giga-bit DRAM"; Technical Digest of IEDM; pages 907-910; December 1995.
_____	AZ	J.K. PARK et al.; "Isolation Merged Bit Line Cell(IMBC) for 1Gb DRAM and Beyond". Technical Digest of IEDM; pages 911-914; December 1995.
_____	BA	
_____	BB	

Examiner	Date Considered